

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) An apparatus for computing the
2 absolute value of a complex number having a real part and an
3 imaginary part, wherein the real and imaginary parts of the complex
4 number are each represented by a digital number of B bits, where B
5 is an integral factor of 4, the apparatus comprising:

6 a first squaring unit having an input receiving said real part
7 of said complex number and an output generating a first square of
8 said real part multiplied with itself;

9 a second squaring unit having an input receiving said
10 imaginary part of said complex number and an output generating a
11 second of said imaginary part multiplied with itself;

12 said first squaring unit and said second squaring unit each
13 include:

14 a first multiplier having a first input receiving a set
15 of B/2 least significant bits of said input, a second input
16 receiving said set of B/2 least significant bits of said input
17 and a product output generating a first product of said B
18 least significant bits multiplied by itself,

19 a second multiplier having a first input receiving a set
20 of B/2 most significant bits of said input, a second input
21 receiving said set of B/2 most significant bits of said input
22 and a product output generating a second product of said B
23 most significant bits multiplied by itself,

24 a third multiplier having a first input receiving said
25 set of B/2 least significant bits of said input, a second
26 input receiving said set of B/2 most significant bits of said
27 input and a product output generating a third product of said

28 B least significant bits multiplied by said B most significant
29 bits,

30 a shift unit having an input receiving said product
31 output of said third multiplier and a shift output generating
32 a left shifted output left shifted by $(B/2)+1$ bits, and

33 a summing unit having a first input having least
34 significant bits receiving said first product and most
35 significant bits receiving said second product, a second input
36 receiving said left shifted output and generating a sum output
37 being a sum of said first and second inputs, said sum output
38 being said output of said squaring unit;

39 said first multiplier of each of said first squaring unit and
40 said second squaring unit includes

41 a fourth multiplier having a tenth input receiving a set
42 of $B/4$ least significant bits of said first input of said
43 corresponding multiplier, a second input receiving said set of
44 $B/4$ least significant bits of said first input of said
45 corresponding multiplier and a product output generating a
46 fourth product of said $B/4$ least significant bits multiplied
47 by itself,

48 a fifth multiplier having a first input receiving a set
49 of $B/4$ most significant bits of said first input of said
50 corresponding multiplier, a second input receiving said set of
51 $B/4$ most significant bits of said first input of said
52 corresponding multiplier and a product output generating a
53 fifth product of said $B/4$ most significant bits multiplied by
54 itself,

55 a sixth multiplier having a first input receiving said
56 set of $B/4$ least significant bits of said first input of said
57 corresponding multiplier, a second input receiving said set of
58 $B/4$ most significant bits of said first input of said
59 corresponding multiplier and a product output generating a

60 sixth product of said B/4 least significant bits multiplied by
61 said B/4 most significant bits,

62 a shift unit having an input receiving said output of
63 said sixth multiplier and a shift output generating an left
64 shifted output left shifted by (B/4)+1 bits, and

65 a summing unit having a first input having least
66 significant bits receiving said third product and most
67 significant bits receiving said fourth product, a second input
68 receiving said left shifted output and generating a sum output
69 being a sum of said first and second inputs, said sum output
70 being said output of said multiplier;

71 a summing unit having a first input receiving said first
72 square, having a second input receiving said second square and an
73 output generating a sum of said first square and said second
74 square; and

75 a square root unit having an input receiving said sum and an
76 output generating a square root of said sum, said square root being
77 said absolute value of said complex number.

2. (Canceled)

1 3. (Currently Amended) The apparatus of claim 2 1, wherein
2 the real and imaginary parts of the complex number are each
3 represented by a signed digital number, and wherein:

4 said first multiplier of each of said first and second
5 squaring units is an unsigned multipliers multiplier;

6 said second and third multipliers of each of said first and
7 second squaring unit are a signed multiplier multipliers; and

8 said summing unit is a signed summing unit.

4 to 8. (Canceled)

1 9. (Currently Amended) ~~The An~~ apparatus of ~~claim 1, wherein~~
2 for computing the absolute value of a complex number having a real
3 part and an imaginary part, the apparatus comprising:

4 a first squaring unit having an input receiving said real part
5 of said complex number and an output generating a first square of
6 said real part multiplied with itself;

7 a second squaring unit having an input receiving said
8 imaginary part of said complex number and an output generating a
9 second of said imaginary part multiplied with itself;

10 a summing unit having a first input receiving said first
11 square, having a second input receiving said second square and an
12 output generating a sum of said first square and said second
13 square; and

14 a square root unit having an input receiving said sum and an
15 output generating a square root of said sum, said square root being
16 said absolute value of said complex number, said square root unit
17 includes including a plurality of processing elements equal in
18 number to a number of bits representing said real part and said
19 imaginary part of said complex number disposed in a cascade chain,
20 each processing element having

21 a current data input, said current data input of a first
22 processing element in said chain receiving said sum output of
23 said summing unit,

24 a current remainder input, said current remainder input
25 of said first processing element in said chain receiving a
26 zero input,

27 a current root input, said current root input of said
28 first processing element in said chain receiving a zero input,

29 a next data output, said next data output connected to
30 said current data input of a next processing element in said
31 chain,

32 a next remainder output, said next remainder output
33 connected to said current remainder input of a next processing
34 element in said chain, said next remainder output of a last
35 processing element in said chain forming a remainder part of
36 said square root,

37 a next root output, said next root output connected to
38 said current root input of a next processing element in said
39 chain, said next root output of said last processing element
40 in said chain forming an integer part of said square root,

41 a shift unit having an input connected to said current
42 data input and an output connected to said next data output,
43 said shift unit left shifting said current data input two
44 bits,

45 a signed summing unit having a positive input receiving
46 as least significant bits two most significant bits of said
47 current data input and bits of said current remainder input
48 left shifted two bits and a negative input having two least
49 significant bits receiving the digital constant "01" and bits
50 receiving said current root input left shifted two bits, said
51 signed summing unit generating a difference output
52 corresponding to a difference of said positive input minus
53 said negative input and a sign bit indicating a sign of said
54 difference,

55 a first multiplexer having a first input receiving as
56 least significant bits two most significant bits of said
57 current data input and bits of said current remainder input
58 left shifted two bits, a second input receiving said
59 difference output, a control input receiving said sign bit and
60 an output coupling a selected one of said first input and said
61 second input dependent upon said control input, said output
62 connected to said next remainder output, and

63 a second multiplexer having a first input receiving as
64 least significant bit a digital constant "0" and bits of said
65 current root input left shifted one bit, a second input
66 receiving as least significant bit a digital constant "1" and
67 bits of said current root input left shifted one bit, a
68 control input receiving said sign bit and an output coupling a
69 selected one of said first input and said second input
70 dependent upon said control input, said output connected to
71 said next root output.

1 10. (Original) The apparatus of claim 9, wherein:
2 each processing element further having
3 a first data latch having an input receiving said shift
4 unit output temporarily storing said next data output,
5 a second data latch having an input receiving said output
6 of said first multiplexer temporarily storing said next
7 remainder output, and
8 a third data latch having an input receiving said output
9 of said second multiplexer temporarily storing said next root
10 output.

1 11. (Original) The apparatus of claim 9, wherein:
2 said square root unit includes
3 at least one processing element disposed in a cascade
4 chain, each processing element having
5 a current data input, said current data input of a
6 first processing element in said chain receiving said sum
7 output of said summing unit,
8 a current remainder input, said current remainder
9 input of said first processing element in said chain
10 receiving a zero input,

11 a current root input, said current root input of
12 said first processing element in said chain receiving a
13 zero input,

14 a next data output, said next data output connected
15 to said current data input of a next processing element
16 in said chain,

17 a next remainder output, said next remainder output
18 connected to said current remainder input of a next
19 processing element in said chain,

20 a next root output, said next root output connected
21 to said current root input of a next processing element
22 in said chain,

23 a shift unit having an input connected to said
24 current data input and an output connected to said next
25 data output, said shift unit left shifting said current
26 data input two bits,

27 a signed summing unit having a positive input
28 receiving as least significant bits two most significant
29 bits of said current data input and bits of said current
30 remainder input left shifted two bits and a negative
31 input having two least significant bits receiving the
32 digital constant "01" and bits receiving said current
33 root input left shifted two bits, said signed summing
34 unit generating a difference output corresponding to a
35 difference of said positive input minus said negative
36 input and a sign bit indicating a sign of said
37 difference,

38 a first multiplexer having a first input receiving
39 as least significant bits two most significant bits of
40 said current data input and bits of said current
41 remainder input left shifted two bits, a second input
42 receiving said difference output, a control input

43 receiving said sign bit and an output coupling a selected
44 one of said first input and said second input dependent
45 upon said control input, said output connected to said
46 next remainder output, and

47 a second multiplexer having a first input receiving
48 as least significant bit a digital constant "0" and bits
49 of said current root input left shifted one bit, a second
50 input receiving as least significant bit a digital
51 constant "1" and bits of said current root input left
52 shifted one bit, a control input receiving said sign bit
53 and an output coupling a selected one of said first input
54 and said second input dependent upon said control input,
55 said output connected to said next root output;

56 a switch having

57 a first data input receiving said sum output of said
58 summing unit,

59 a second data input receiving said next data output
60 of a last processing element in said chain,

61 a remainder input receiving said next remainder
62 output of said last processing element in said chain,

63 a root input receiving said next root output of said
64 last processing element in said chain,

65 a data output connected to said current data input
66 of a first processing element in said chain,

67 a first remainder output connected to said current
68 remainder input of said first processing element in said
69 chain,

70 a first root output connected to said current root
71 of said first processing element in said chain,

72 a second remainder output a remainder part of said
73 square root, and

74 a second root output forming an integer part of said
75 square root,
76 said switch having a first state connecting said first
77 input data to said data output, a digital constant "0" to said
78 first remainder output, a digital constant "0" to said first
79 root output and said root input to said second root output,
80 said switch having a second state connecting said second
81 data input to said data output, said remainder input to said
82 first remainder output and said root input to said first root
83 output; and
84 a loop control connected to said switch, said loop
85 control controlling said first and second states of said
86 switch to input data to said chain of processing elements,
87 recirculate said data, remainder and root from said last
88 processing element in said chain to said first processing
89 element in said chain at least once, and output a calculated
90 root.

1 12. (Original) The apparatus of claim 11, wherein:
2 said first state of said switch further connects said
3 remainder input to said remainder output.

1 13. (Original) The apparatus of claim 11, wherein:
2 each processing element further having
3 a first data latch having an input receiving said shift
4 unit output temporarily storing said next data output,
5 a second data latch having an input receiving said output
6 of said first multiplexer temporarily storing said next
7 remainder output, and
8 a third data latch having an input receiving said output
9 of said second multiplexer temporarily storing said next root
10 output.